Fig.1

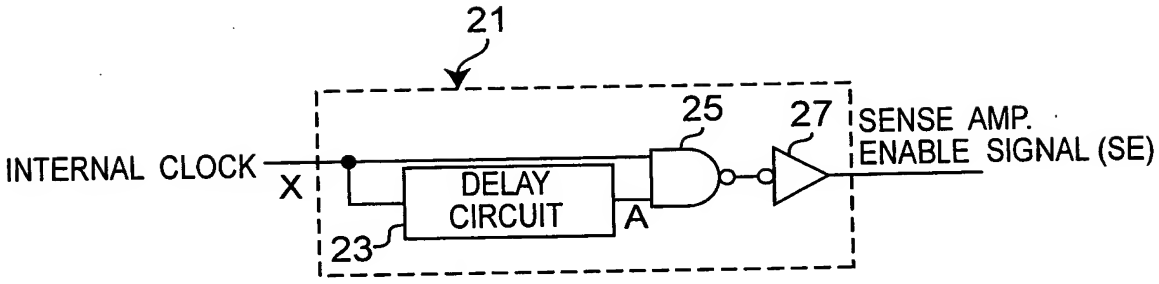

21
25
27
SENSE AMP.
ENABLE SIGNAL (SE)
INTERNAL CLOCK
X
DELAY
CIRCUIT
A
23

Fig.2

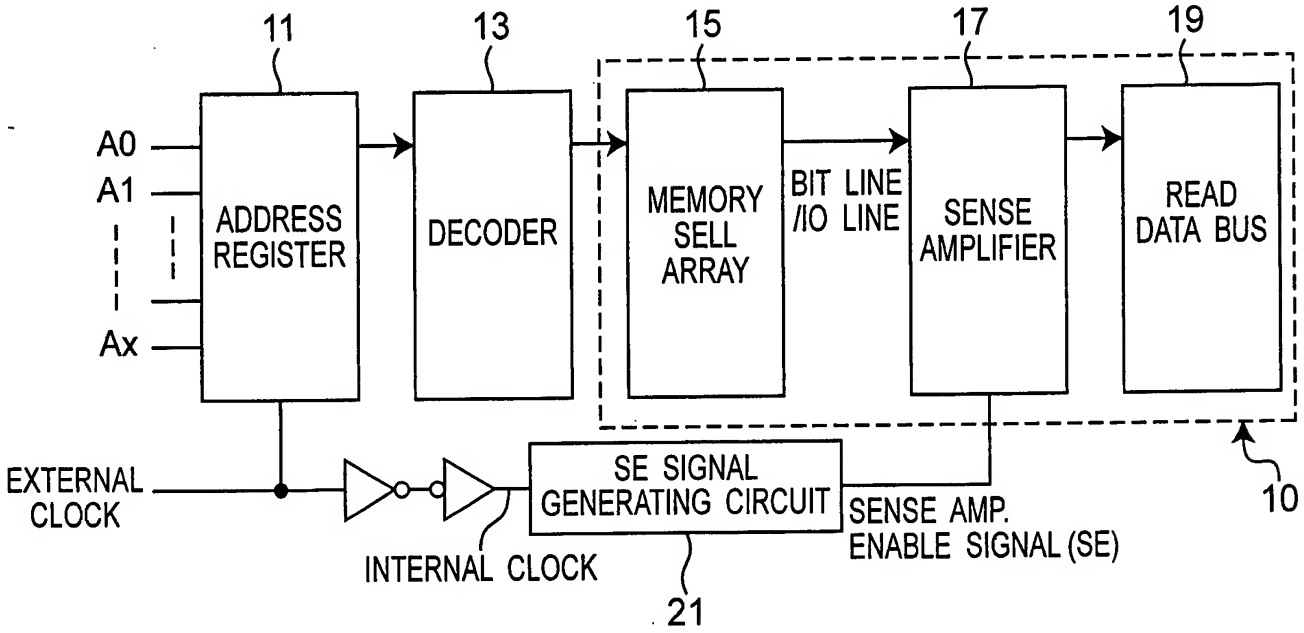

11
13
15
17
19
A0
A1
Ax
ADDRESS REGISTER
DECODER
MEMORY SELL ARRAY
BIT LINE /IO LINE
SENSE AMPLIFIER
READ DATA BUS
EXTERNAL CLOCK
SE SIGNAL GENERATING CIRCUIT
SENSE AMP. ENABLE SIGNAL (SE)
INTERNAL CLOCK
10
21

Fig.3

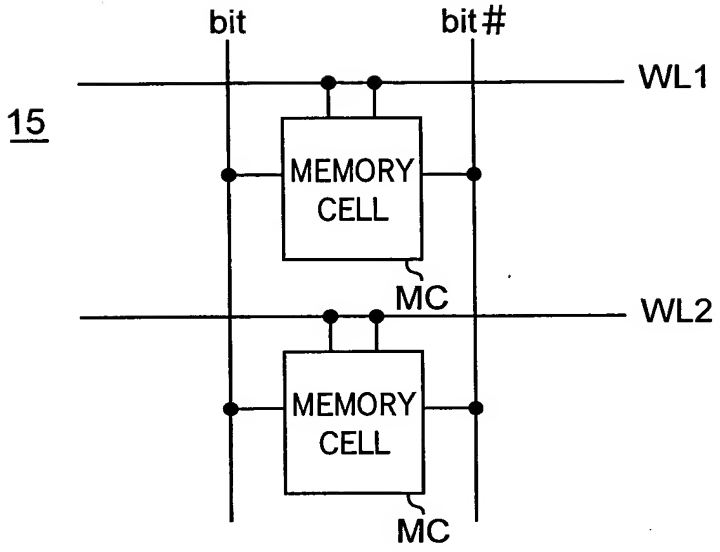
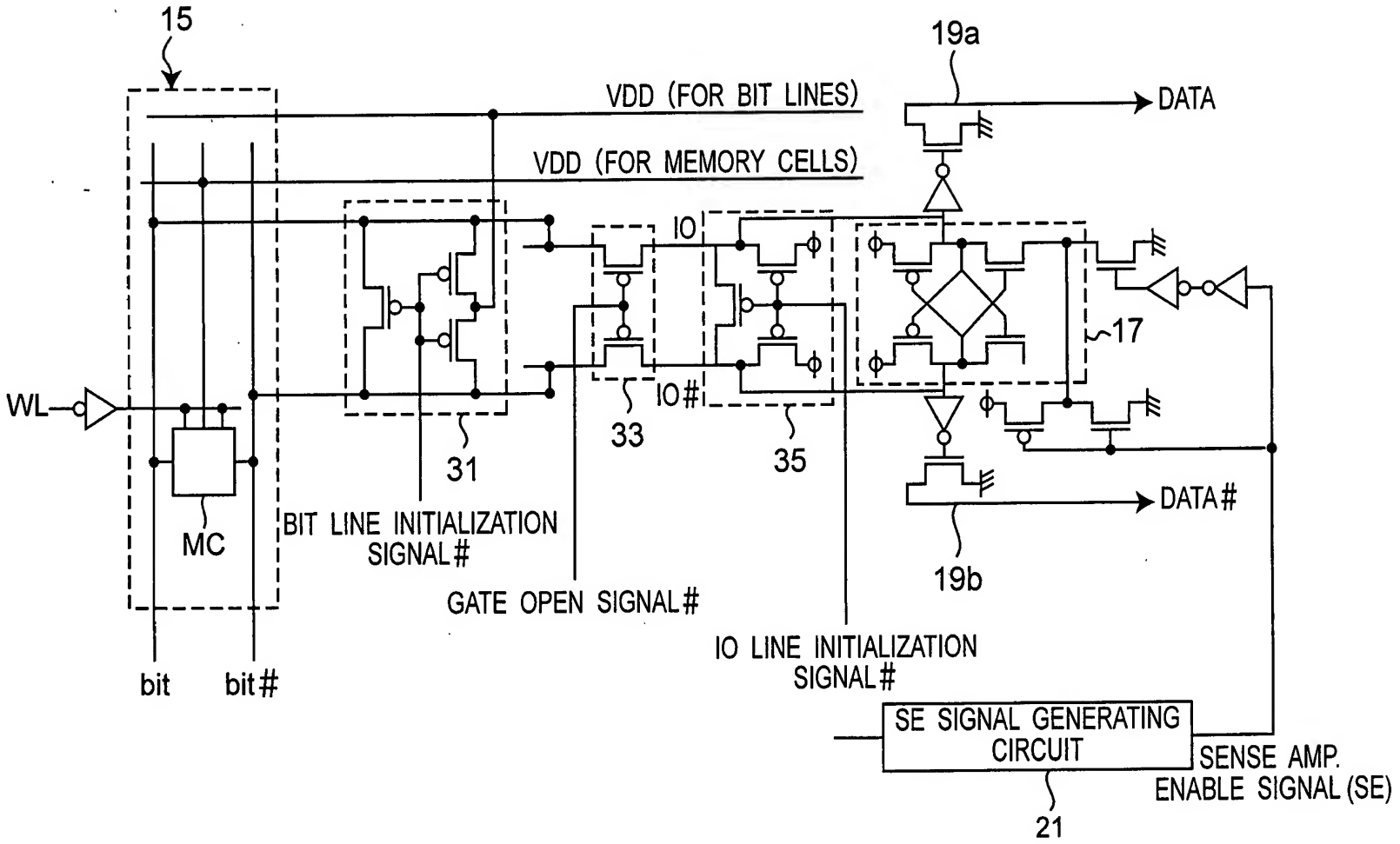


Fig.4


15
19a
VDD (FOR BIT LINES)
DATA
VDD (FOR MEMORY CELLS)
IO
17
WL
IO#
33
35
31
DATA#
MC
BIT LINE INITIALIZATION SIGNAL#
19b
GATE OPEN SIGNAL#
IO LINE INITIALIZATION SIGNAL#
bit
bit#
SE SIGNAL GENERATING CIRCUIT
SENSE AMP. ENABLE SIGNAL (SE)
21

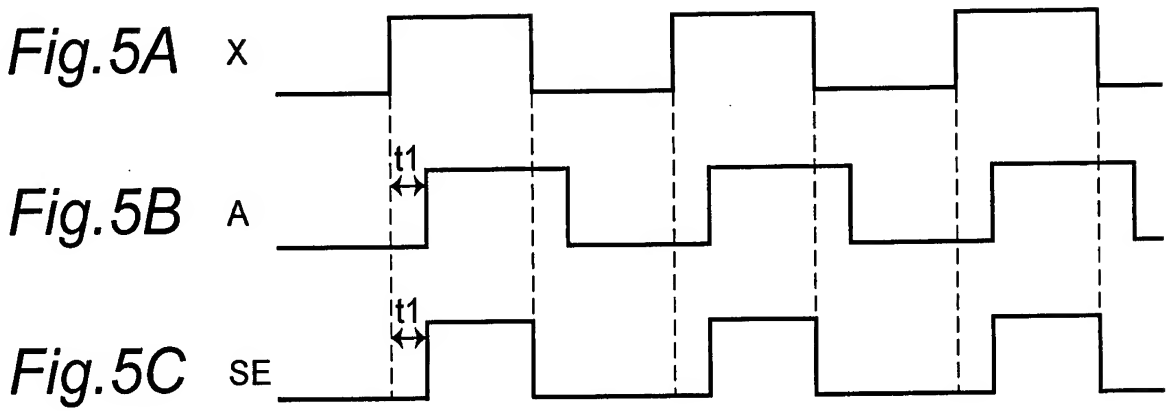


Fig.5A
X
t1
Fig.5B
A
t1
Fig.5C
SE

Fig.6A

WL1

Fig.6B

WL2

Fig.6C

BIT LINES

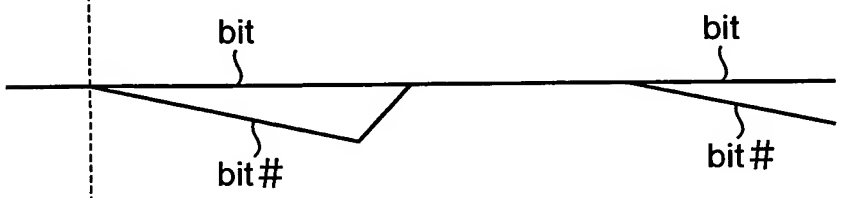


Fig.6D

BIT LINE INITIALIZATION SIGNAL#

Fig.6E

EXTERNAL CLOCK

Fig.6F

INTERNAL CLOCK

Fig.6G

INTERNAL CLOCK (DELAY)

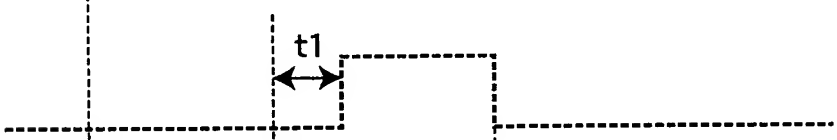


Fig.6H

SENSE AMP. ENABLE SIGNAL

Fig.6I

IO LINE INITIALIZATION SIGNAL#

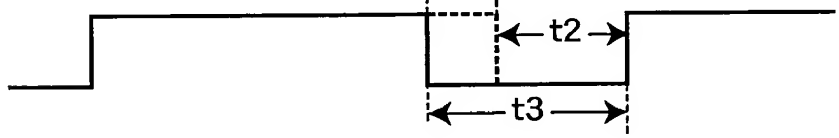
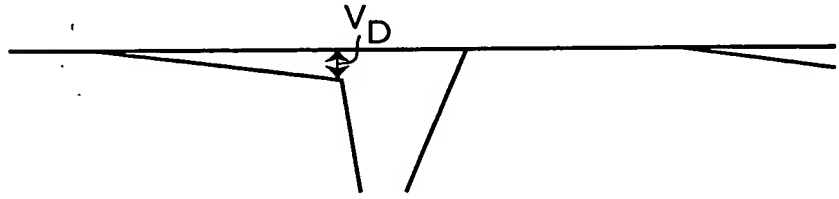


Fig.6J

IO LINES



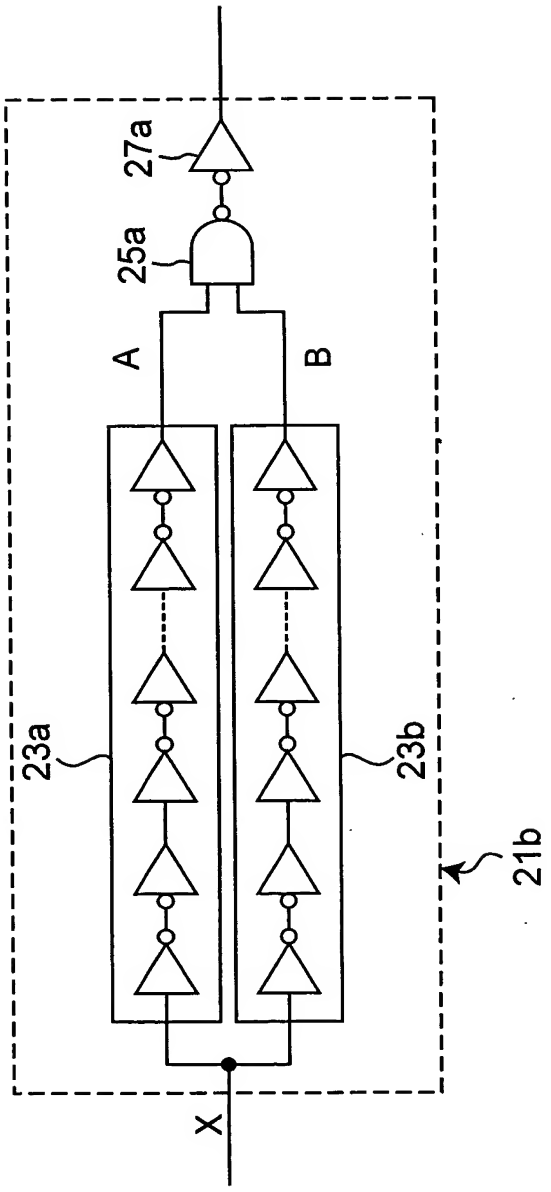


Fig.7

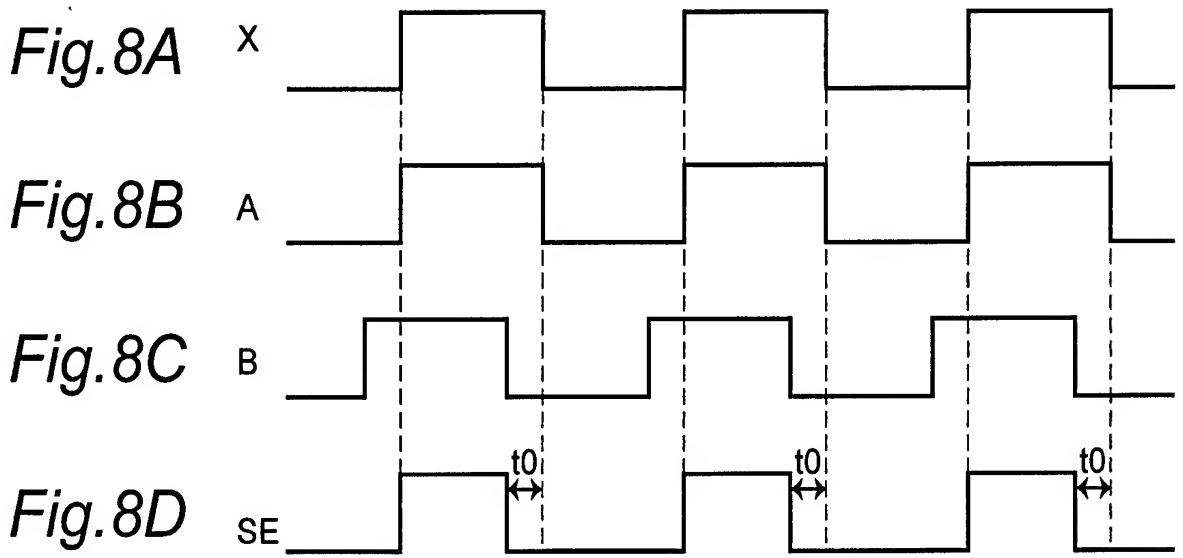


Fig.8A
X
Fig.8B
A
Fig.8C
B
Fig.8D
SE
t0
t0
t0

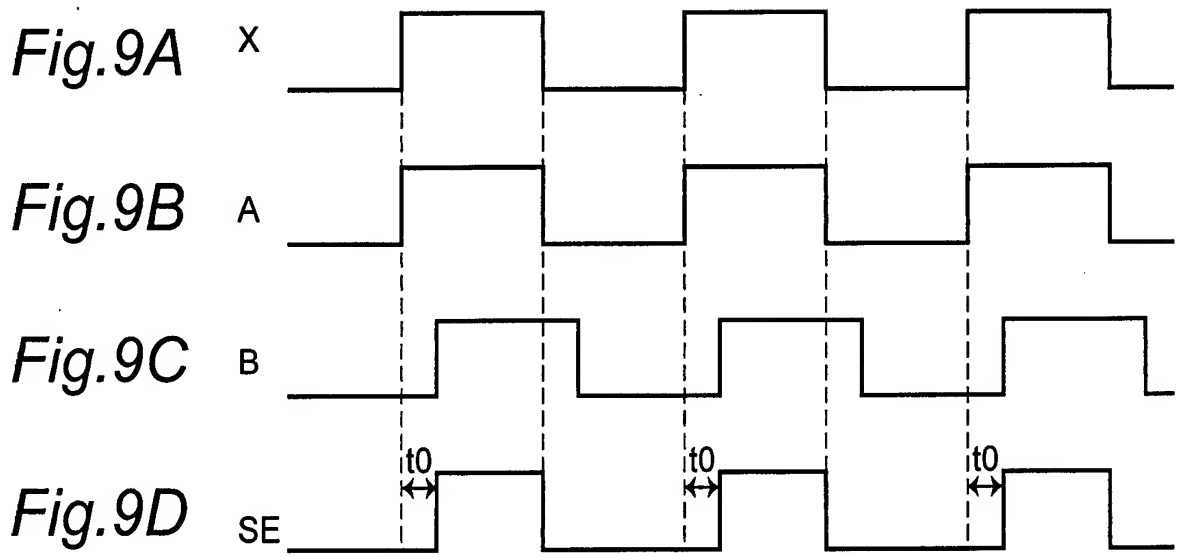


Fig.9A
X
Fig.9B
A
Fig.9C
B
Fig.9D
SE
t0
t0
t0